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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,041	04/08/2004	Kiran V. Chatty	BUR920030188US1	3040

42221 7590 03/21/2007

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,041	CHATTY ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on December 18, 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figure 2B (APAF) in view of Ker et al. (US Pub. 2002/0122280 A1) and Amano et al. (US 6,194,776).

In re claim 1, the APAF 2B shows an ESD NMOSFET comprising : a substrate having first (37), second (31) and third wells (38) formed in said substrate, and separated by shallow well isolation regions (33 and 34) generally separating the bottom of said second well from said substrate with a conductive band (40); a source (25) and drain (26) region in said second well forming an FET, said drain being connected to an I/0 pad (11) for protecting said pad against an ESD event; and a path of substrate material to increase the substrate resistance in the path of the current which flows through said I/0 pad to a substrate contact (30) and drain (26) during an ESD event. The first and third wells are completely isolated from the drain and source (by isolation regions (33 and 34). The APAF shows all of the elements of the claims except the

segmented conductive band, the path of substrate material extending through an opening in the conductive band region, and electrically connecting the second well to the substrate. Ker et al. shows (fig. 5) an ESD protection device having first (60), second (40), and third (42) wells formed in a substrate. The first and third wells are connected along a bottom with a conductive band region (3201 and 3202). The conductive band region is segmented and has an opening through which a path of the substrate material extends through it so that the second well (40) is connected to the substrate. The substrate contact (36) is located outside the first and third wells. With this configuration, the p-well is partially connected to the substrate, the resistance is increased in that region, and the device is turned on more quickly [0047]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conductive band region of the APAF by forming an opening in the conductive band as taught by Ker to increase the resistance in the path between the p-well and the common substrate, which would ultimately increase the trigger speed of the device.

The APAF and Ker show all of the elements of the claims except the substrate contact being located outside the first, second, and third wells and directly connected to the substrate. Amano et al. shows (fig. 1) a MOSFET formed in a triple well structure in which the substrate contact (4) is formed outside the first, second, and third wells (1W, 2, 1W) and directly connected to the substrate. The first and third wells (1W left and right) are completely isolated from the drain source and substrate contact (by isolation region14b). With this configuration potential is uniformly supplied from the substrate to

the well region without forming the contact in the well region. By forming the contact outside the well region, the size of the device can be reduced while satisfying the original operating effects of the triple well structure (col. 9, lines 27-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of the APAF and Ker by forming the substrate contact outside the well structure as taught by Amano to reduce the size of the device while maintaining the original triple well effects.

In re claim 3, the APAF 2B shows that said first and third wells are N-wells and said conductive band region comprises a semiconductor region which is N doped.

In re claim 4, Ker shows (fig. 5) that said conductive band region is segmented forming the resistive path to said substrate.

In re claim 5, the APAF 2B shows that said FET has a gate (27) connection and source (25) connected to said substrate contact (30).

In re claim 6, the combined references inherently show that said drain is connected through a matching impedance to said I/0 pad to provide a signal from a circuit on said substrate to said I/0 pad because the structure and materials are the same as the instant invention.

In re claim 13, the APAF 2B shows an ESD NMOSFET comprising: a substrate having first (31), second (37) and third wells (38) formed in said substrate, said first well comprising a P-well (31) separated from second and third N-wells by shallow well isolation regions (33 and 34), said first well separated from said substrate along a bottom thereof with a conductive band region (40); a substrate contact (30); a source

(25) and drain (26) region in said P-well forming a FET, said drain being connected to an I/0 pad (11) for protecting said pad against an ESD event; and a resistive path (29) extending through the P-well which decreases the trigger voltage for the FET. The first and third wells are completely isolated from the drain and source of the MOSFET (by the isolation regions 33 and 34). The APAF shows all of the elements of the claims except the substrate contact outside of the first, second and third wells, and the resistive path extending through an opening in the segmented conductive band region. Ker et al. shows (fig. 5) an ESD protection device having first (60), second (42), and third (40) wells formed in a substrate. The first and third wells are connected along a bottom with a conductive band region (3201 and 3202) and separate the first P-well from the substrate. The conductive band region has an opening through which a path of the substrate material extends through it. A substrate contact (p+ region connected to P-well 36) is formed outside of the first, second, and third wells. With this configuration, the p-well is partially connected to the substrate, the resistance is increased in that region, and the device is turned on more quickly [0047]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conductive band region of the APAF by forming an opening in the conductive band as taught by Ker to increase the resistance in the path between the p-well and the common substrate, which would ultimately increase the trigger speed of the device.

The APAF and Ker show all of the elements of the claims except the substrate contact being located outside the first, second, and third wells and directly connected to the substrate. Amano et al. shows (fig. 1) a MOSFET formed in a triple well structure in

which the substrate contact (4) is formed outside the first, second, and third wells (1W, 2, 1W) and directly connected to the substrate. The first and third wells (1W left and right) are completely isolated from the drain source and substrate contact (by isolation region14b). With this configuration potential is uniformly supplied from the substrate to the well region without forming the contact in the well region. By forming the contact outside the well region, the size of the device can be reduced while satisfying the original operating effects of the triple well structure (col. 9, lines 27-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact structure of the APAF and Ker by forming the substrate contact outside the well structure as taught by Amano to reduce the size of the device while maintaining the original triple well effects.

In re claim 14, the APAF 2B shows that said FET source (25) and gate (27) are connected to the substrate contact (30).

In re claim 15, the APAF 2B shows that said source (25) is connected to said substrate contact (30).

Claims 7, 8, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figure 2B (APAF) in view of Ker et al. (US 6,566,715 B1).

In re claim 7, the APAF 2B discloses [0024-0025] a method for decreasing the trigger voltage of an ESD NMOSFET comprising: locating said ESD NMOSFET in a well of a triple well CMOS structure, and connecting said ESD NFET to an I/0 pad (11);

and providing a resistive path (29) from said first well to a substrate contact (30), whereby the trigger voltage of the said ESD NMOSFET is reduced due to said resistive path between said substrate contact and said I/0 pad. The first, second, and third wells are formed in a substrate of the triple well CMOS structure, the first and third wells are completely isolated from a drain (26) and source (25) of the ESD MOSFET. The APAF shows all of the elements of the claims except the contact being located outside of the triple well structure. Ker et al. discloses (col. 4, lines 6-50 and fig. 5B) a method for improving ESD protection by providing a resistive path (32') from the well of the MOS structure to a contact (46) formed outside one of the N-wells (44) of a triple well structure (44, 32, 44). The resistive path is directly connected to the substrate. The substrate contact is located outside of the first, second, and third wells (44, 32, 44) and is completely isolated from the drain and source of the device (by the isolation 42). With this configuration, the resistance in the conductive path is increase, ultimately improving the ESD performance (col. 4, lines 44-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the resistive path of the APAF by providing a longer path around one of the N-wells of the triple well structure as taught by Ker to increase the resistance and ultimately improve the ESD performance.

In re claim 8, Ker et al. shows (fig. 5 B) that said resistive path is an opening in said well to form a connection between said NMOSFET and said substrate contact.

In re claim 10, the APAF 2B discloses that said ESD NMOSFET further comprises connecting a gate connection and a source of said NMOSFET contact to said substrate.

In re claim 11, as far as understood, the APAF 2B shows that a second and third well of said triple well structure are N-wells, and one of said N-wells is connected to a voltage (Vdd).

In re claim 12, the APAF 2B discloses that the method of connecting a gate of said NMOSFET to said substrate contact.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Figure 2B (APAF) in view of Ker et al. (US 6,566,715 B1) as applied to claim 7 above, and further in view of Ker et al. (US Pub. 2002/0122280 A1).

In re claim 9, the APAF and Ker '715 show all of the elements of the claims except the said well being a P-well with an N-band of N doped semiconductor material which separates said P-well from said substrate, and which includes an opening forming said resistive path. Ker et al. (Pub. '280) shows (fig. 5) an ESD protection device having first (60), second (42), and third (40) wells formed in a substrate. The first and third wells are connected along a bottom with a conductive band region (3201 and 3202). The conductive band region has an opening through which a path of the substrate material extends through it. With this configuration, the p-well is partially connected to the substrate, the resistance is increased in that region, and the device is turned on more quickly [0047]. Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify the conductive band region of the APAF and Ker '715 by forming an opening in the conductive band as taught by Ker "280 to increase the resistance in the path between the p-well and the common substrate, which would ultimately increase the trigger speed of the device.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-6 and 13-15 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 7-12 have been fully considered but they are not persuasive. The applicant primarily asserts that the prior art references do not show all of the elements of the claim, specifically that Ker II (US 6,566,715) does not cure the deficiencies of the APAF. The examiner believes that Ker II properly cures the deficiencies of the APAF. As stated in the rejection above, the APAF only fails to disclose that the substrate contact is located outside the first, second, and third wells and that the resistive path is provided from the well of the triple well to the substrate contact located outside of the triple well. The applicant's argues that Ker II discloses that the n-well (44) partially overlays the n+ doped region (38) and thus implies that Ker II does not disclose that the first and third wells are not completely isolated from the source and drain for this reason. However, such an argument is irrelevant since the APAF 2B already shows that the first and third wells (37, 38) are already completely isolated from the source and drains (25, 26) by isolation regions (34, 33). It does not matter that Ker II shows that the n-well (44) is electrically connected to the source/drain

region. Ker II was only cited to show that the substrate contact (46) is located outside of the first and third wells (44) and that a resistive path (32') is provided from the well (32) to the substrate contact (50) which is shown in figure 5B. Therefore, the combined references show all of the elements of the claims and the rejection is still proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren
March 13, 2007